

# Christopher Lu

---

|                     |  |   |
|---------------------|--|---|
| Contact Information | 25 Rio Robles East<br>Unit 301<br>San Jose, CA 95134   | <i>Phone:</i> (508) 404-9889<br><i>E-mail:</i> chris@lulabs.net<br><i>WWW:</i> www.lulabs.net |
| Education           | BS in Computer Science, Carnegie Mellon University, Pittsburgh, PA<br>Expected graduation date: May 2010<br>Major QPA: 3.7   |   |
| Expertise           | <ul style="list-style-type: none"><li>• Programming: C, Standard ML, {x86, MIPS, Z80} assembly, Verilog</li><li>• Software: gcc, git, Linux build toolchain</li><li>• Hardware: USB, computer graphics</li></ul>   |   |
| Experience          | <b>IVA Corporation</b> , Sudbury, MA<br><br><i>Intern</i> 6/2009 - 8/2009 <ul style="list-style-type: none"><li>• Wrote firmware for Cypress FX2-based USB Video Class (UVC) cameras.</li><li>• Developed an efficient algorithm to buffer data for JPEG DCT transformation.</li><li>• Gained experience with USB, UVC, and 8051 microcontrollers.</li></ul><br><b>Carnegie Mellon University</b> , Pittsburgh, PA<br><br><i>Teaching Assistant</i> 9/2008 - 12/2008 <ul style="list-style-type: none"><li>• Assisted 15-213 (Introduction to Computer Systems) course staff.</li><li>• Taught students various systems programming fundamentals.</li></ul><br><b>Analog Devices</b> , Wilmington, MA<br><br><i>Intern</i> , Digital Imaging Systems Group 6/2008 - 8/2008 <ul style="list-style-type: none"><li>• Maintained datatool, an in-house program to analyze and visualize wafer test data. Extended it with multiple wafer capability and analysis.</li><li>• Gained experience with large software projects.</li></ul><br><i>Intern</i> , Digital Imaging Systems Group 6/2007 - 8/2007 <ul style="list-style-type: none"><li>• Designed and implemented an FPGA-based data timing generator to replace the Tektronix HFS9003 stimulus system as part of a standard CCD driver test setup.</li><li>• Tested CCD drivers and gained knowledge of CCD operation and test parameters.</li><li>• Devised a systematic organization scheme for test data.</li></ul> |   |
| Projects            | <b>'FireARM' ARM CPU</b> <ul style="list-style-type: none"><li>• Implemented a pipelined ARM-compatible CPU core in Verilog, with cache.</li></ul><br><b>MandelFPGA</b> <ul style="list-style-type: none"><li>• Designed and implemented a computational pipeline to interactively display a Mandelbrot fractal on a VGA monitor in real time, using an FPGA.</li></ul>  |   |
| Coursework          | <ul style="list-style-type: none"><li>• 15-410, Operating Systems Design and Implementation</li><li>• 18-447, Introduction to Computer Architecture</li><li>• 15-312, Principles of Programming Languages</li><li>• 15-411, Compiler Design</li></ul>  |   |